REMARKS

The Applicants respectfully request reconsideration and allowance of Claims 1 through 18 in view of the above amendments and the following arguments.

It is noted that the First Office Action included no prior art based rejection as to Claims 18 through 20. The Applicant thus assumes that these claims are directed to allowable subject matter.

EXAMINER INTERVIEW SUMMARY

The Applicants appreciate the telephone interview conducted with the undersigned attorney on June 17, 2003. In the interview, the undersigned attorney described the above technical corrections to Claims 12 and 18 to properly refer to the intended circuit devices. The undersigned attorney also described the above amendment to Claim 18 to incorporate the limitation previously set out in Claim 20. The telephone interview further included a discussion of elements (g) and (h) of Claim 1 and the differences between those claim elements and the processes described in the references of record in this case. The Examiner requested additional comments on U.S. Patent No. 5,266,821 in view of the disclosure at claim 1 of that patent. The interview was conducted primarily to address any questions the Examiner may have had on the proposed response and thus did not result in an agreement as to allowability.

THE AMENDMENTS

Claim 12 is amended to eliminate the technically incorrect reference to "additional circuit device" and "additional device bodies." In the present invention, the capacitor device bodies correspond to device bodies for a first type of circuit device and the capacitor structure lateral regions correspond to the source and drain regions for a second type of circuit device. Claim 12

is amended to reflect this arrangement and the claims depending from Claim 12 are amended accordingly for consistency with Claim 12.

Claim 18 is amended similarly to Claim 12 and further amended to incorporate the limitation previously set out in Claim 20.

The disclosure is amended at page 1 to add the patent number for the related application, and amended at pages 10 and 11 to add language consistent with that used in the amended claims.

THE CLAIM OBJECTIONS AND SECTION 112 REJECTIONS

The Examiner objected to Claims 12 through 20 under 37 C.F.R. §1.75(d)(1) and rejected the same claims for indefiniteness under 35 U.S.C. §112, second paragraph in light of the inadvertent technical error described above. The Applicants submit that the above claim amendments for technical consistency with the disclosure eliminate the grounds for objection under 37 C.F.R. §1.75(d)(1) and grounds for rejection under 35 U.S.C. §112, second paragraph.

CLAIM 18 IS NOT ANTICIPATED BY THE YAMAGUCHI PATENT

The Examiner rejected Claims 18-19 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,576,565 to Yamaguchi (the "Yamaguchi patent"). The Applicants respectfully submit that claim 18 as amended is not anticipated by the Yamaguchi reference and is entitled to allowance.

Claim 18 is amended above to incorporate the limitation previously set out in claim 20, which was not rejected on prior art grounds in the office action mailed March 28, 2003. The Applicants submit that the prior art of record does not anticipate or suggest the step of adding additional impurity in the capacitor device body in a silicon-on-insulator circuit. Thus, the

Applicants believe that Claim 18 is entitled to allowance.

CLAIMS 1 THROUGH 17 ARE NOT OBVIOUS IN VIEW OF THE CITED REFERENCES

The Examiner rejected Claims 1 through 14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,266,821 to Chern (the "821 patent") in view of one or more additional references. The Applicants respectfully submit that the claims are not obvious over the cited references and are entitled to allowance.

It is noted that Claims 15 through 17 were not rejected on prior art. The Applicants thus presume that Claims 15 through 17 were found in the first Office Action to be directed to allowable subject matter.

Independent Claims 1 and 12 are both directed to a method of forming a capacitor on a semiconductor substrate. Among its other requirements, Claim 1 requires the following steps:

(g) electrically connecting the first and second lateral regions to a first supply voltage potential at a first longitudinal end of the device body; and

(h) electrically connecting the electrode layer to a second supply voltage potential at a second longitudinal end of the device body opposite to the first longitudinal end of the device body.

Independent Claim 12 includes similar limitations at elements (f) and (g). The Applicants submit that none of the references of record in this case teach or suggest the step of electrically connecting the capacitor device lateral regions to a the respective voltage at a longitudinal end of the device body opposite to the end at which the electrode is connected.

The primary reference cited in the section 103 rejections, the 821 patent, discloses a basic capacitor structure similar to that set out in the present application. However, the 821 patent does not teach or suggest the connecting steps set out in Claim 1 and Claim 12. In contrast to the

connecting steps set out in the present claims, Figure 9 of the 821 patent merely shows a diagrammatic electrical connection between the lateral N+ regions in the capacitor structure and ground. Figure 8 of the 821 patent appears to show Vss connections at outside of the N-well of the device structure. Although this may be an error in the drawing, the reference does not in any event teach or suggest the electrical connection to lateral regions as set out in Claims 1 and 12.

In the above-described telephone interview, the Examiner suggested that the disclosure set out in Claim 1 of the 821 patent might be construed as describing the electrical connection steps set out in Claims 1 and 12 of the present invention. However, Claim 1 of the 821 patent merely discloses that bottom plate of the capacitor includes a doped region of the substrate (the N-well shown in Figure 9 of the 821 patent) and "with contacts of the bottom plate including a portion of the substrate, said portion being further doped to be more heavily doped ...." It is believed that this reference to contacts simply refers to the N+ regions shown in Figure 9 of the 821 patent, but does not disclose where the electrical contacts to those regions are located specifically. The Examiner also suggested that Figure 8 of the 821 patent is mislabeled and that the N-well in the structure in fact comprises the solid rectangle rather than the dashed rectangle actually shown in the drawing. However, even assuming this is the case and assuming the small solid squares represent vias for electrical coupling to Vss, Figure 8 of the 821 patent shows electrical coupling to the N-well and not the lateral regions defined by the N+ material shown in Figure 9.

None of the secondary references cited in the section 103 rejections make up for this basic deficiency regarding the 821 patent. U.S. patent No. 4,929,989 to Hayano (the "989 patent") was cited for showing the application of an insulating layer over the capacitor electrode and lateral regions. However, the 989 patent does not teach or suggest the electrical connection steps as set out at elements (g) and (h) of Claim 1 and elements (f) and (g) of Claim 12. The

other secondary references cited in the section 103 rejections, U.S. patent Nos. 6,018,175, 5,965, 928, and 6,034,388 also do not teach or suggest the connecting steps required in Claims 1 and 12.

Because the cited references do not teach or suggest the electrical connection steps set out in Claims 1 (elements (g) and (h)) and 12 (elements (f) and (g)), the Applicants respectfully submit that the claims are not obvious in view of the cited references and are entitled to allowance together with their respective dependent claims.

CONCLUSION

For all of the above reasons and in view of the claim amendments, the Applicants respectfully request reconsideration and allowance of Claims 1 through 18.

If the Examiner should feel that any issue remains as to the allowability of these claims, or that a conference might expedite allowance of the claims, he is asked to telephone the undersigned attorney.

Respectfully submitted,

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Dated: June 19, 2003

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CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, (Fax No. 703-872-9318) on June 19, 2003.

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